

## CLAIMS

What is Claimed is:

1. A timer circuit comprising:

5 an output stage coupled to a configurable delay element; and  
a pull-down path coupled to said output stage and comprising a circuit for  
providing a selectable amount of pull down current, said pull-down path also  
coupled to receive a reference signal that varies in proportion to temperature  
and wherein a delay through said timer circuit is inversely proportional to said  
10 temperature.

2. A timer circuit as described in Claim 1 wherein said reference  
signal is derived from a band gap reference circuit.

15 3. A timer circuit as described in Claim 2 wherein said reference  
signal is a VPTAT voltage signal.

4. A timer circuit as described in Claim 1 wherein said configurable  
delay element comprises a plurality of gated capacitors which can be  
20 selectively coupled to said output stage via a plurality of corresponding pass  
gates.

5. A timer circuit as described in Claim 4 wherein said configurable  
delay element further comprises a plurality of configuration bits each for  
25 controlling a respective pass gate.

6. A timer circuit as described in Claim 1 wherein said circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel wherein each gated pull-down  
5 circuit comprises a first transistor having a gate controlled by a respective configuration bit and a series coupled second transistor having a gate controlled by said reference signal.

7. A timer circuit as described in Claim 4 wherein said circuit for  
10 providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel wherein each gated pull-down circuit comprises a first transistor having a gate controlled by a respective configuration bit and a series coupled second transistor having a gate controlled by said reference signal.

15 8. A timer circuit as described in Claim 6 wherein said configurable delay element comprises a plurality of gated capacitors which can be selectively coupled to said output stage via a plurality of corresponding pass gates.

20 9. A timer circuit as described in Claim 8 wherein said configurable delay element further comprises a plurality of configuration bits each for controlling a respective pass gate.

10. An electronic device comprising a timer circuit and wherein said timer circuit comprises:

an output stage coupled to a configurable delay element; and

a pull-down path coupled to said output stage and comprising a circuit for  
5 providing a selectable amount of pull down current, said pull-down path also  
coupled to receive a reference signal that varies in proportion to temperature  
and wherein a delay through said timer circuit is inversely proportional to said  
temperature and wherein said reference signal is derived from a band gap  
reference circuit.

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11. An electronic device as described in Claim 10 wherein said  
reference signal is a VPTAT voltage signal.

12. An electronic device as described in Claim 10 wherein said  
15 configurable delay element comprises a plurality of gated capacitors which can  
be selectively coupled to said output stage via a plurality of corresponding pass  
gates.

13. An electronic device as described in Claim 10 wherein said circuit  
20 for providing a selectable amount of pull down current comprises a plurality of  
gated pull-down circuits coupled in parallel wherein each gated pull-down  
circuit comprises a first transistor controlled by a respective configuration bit and  
a series coupled second transistor having a gate controlled by said reference  
signal.

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14. An electronic device as described in Claim 13 wherein said configurable delay element comprises a plurality of gated capacitors which can be selectively coupled to said output path via a plurality of corresponding pass gates.

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15. An electronic device as described in Claim 10 wherein said electronic device is a memory circuit.

16. An electronic device as described in Claim 10 wherein said  
10 electronic device is a write back timer of a memory circuit.

17. A method of varying a delay of a timer circuit comprising:  
during configuration of said timer circuit, setting a first plurality of  
configuration bits which control the amount of elements coupled to an output  
15 stage of said timer circuit to set an amount of delay through said timer circuit;  
during said configuration, setting a second plurality of configuration bits  
which control an amount of pull down current through a pull down path of said  
timer circuit to set an amount of delay through said timer circuit, said pull down  
path coupled to said output stage; and  
20 during operation of said timer circuit, varying a reference signal coupled  
to said pull down path to vary delay through said timer circuit inversely  
proportional to temperature of said timer circuit.

18. A method as described in Claim 17 wherein said reference signal is generated by a band gap circuit and varies proportionally with said temperature.

5 19. A method as described in Claim 18 wherein said pull down path comprises a plurality of parallel coupled pull down circuits, each pull down circuit comprising a first transistor coupled to a respective configuration bit of said second set of configuration bits and a second transistor having a gate coupled to said reference signal.

10 20. A method as described in Claim 19 wherein said elements are gated capacitors which can be selectively coupled to said output stage based on said first set of configuration bits.

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